Thin Film High-Density Integration (HDI) Design Guidelines

Abstract

The design of single- or double-sided Thin Film high density multi-layer substrates depends on a wide range of rules. This paper is intended to be a comprehensive roadmap of the design process, with a focus on the selection of materials, films, and extensive range of options. The purpose is to educate the circuit user on Thin Film High Density Interconnects (HDI) and the benefits of design performance. These benefits are achieved through enhanced control of impedance signal routing, size, noise, and response conditioning using Thin Film design concepts. This paper reviews the flow selection and critical decisions needed to use HDI technology.

Introduction

High-Density Integration products can be a complicated process for design engineers. This guideline has been written to simplify the design process by providing a useful tool to the engineering community. Whether the requirements are for simple resistor networks, integrated resistor-capacitor networks, multilayer components, custom thin film networks on Alumina (Al2O3), Aluminum Nitride (AIN) or Beryllium Oxide (BeO), or substrates requiring special shapes, vias, and unique patterning for microwave applications, this guideline provides the user with a tool to facilitate the design process.

The wide array of thin film capabilities provides solutions for applications serving many markets, including military, automotive, instrumentation-microwave, telecommunications/CATV/fiber optic, wireless, aerospace, and medical.

Selection Roadmap

The design process begins with the engineer reviewing all the options available to achieve a balanced effective layout, and selecting the best fit in terms of substrate choices, metallization schemes, and interconnection technology. Generally the design process works from the substrate up or out so the first choice would be the substrate. From here the first metal layer is designed, making all the major routing connections. Next, any resistors must be placed, giving considerations to power required and the cell size consumed. All resistors should be placed on the substrate surface either front side or back. If front-to- back routing seems appropriate, then through-hole considerations must be addressed as either solid-filled or plated-through.

Next, considerations for placement of other types of components must be addressed. Capacitors, air crossover, and Lange couples must be integrated into the circuit using additional layer routings as required. Figure 1 provides a pictorial view of the selection process.

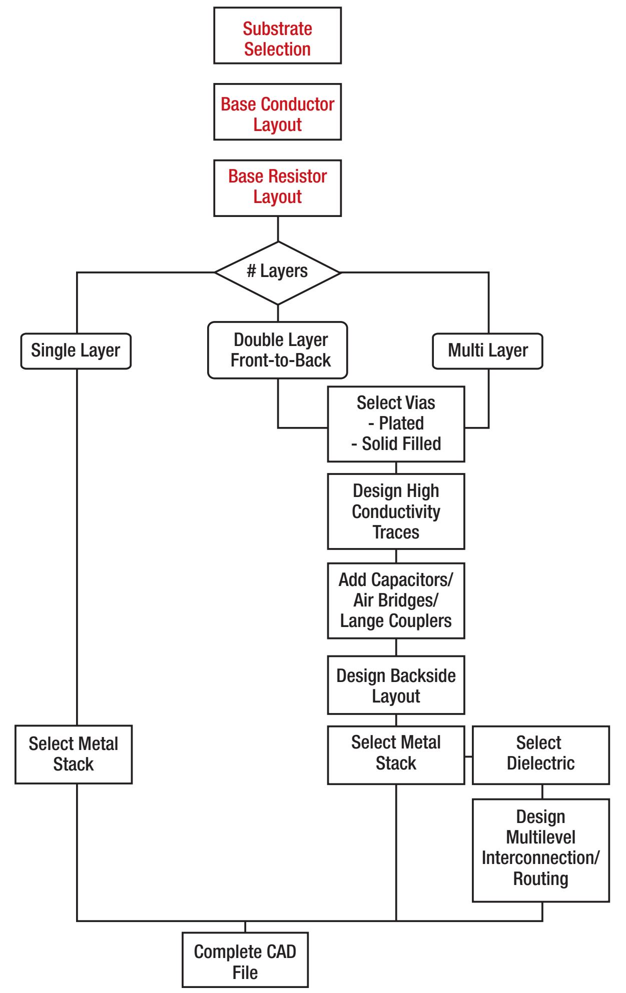

Figure 1. Selection roadmap

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Substrate Characterization

One of the most critical choices in any circuit is the base material on which the circuit is built. As in all designs, the application (Table 1) largely drives the base requirements. The substrate characterization table (Table 2) summarizes many of these choices. Among the primary considerations is the power dissipation required for the circuit. For DC circuits this is a simple choice, but for applications requiring higher frequencies the dielectric constant becomes paramount when frequency response becomes a major consideration. The mechanical properties table (Table 2) summarizes basic characteristics of all the materials compatible with the Vishay process.

Substrates

Material	Uses	Benefits
Alumina (A1203)	Standard hybrid or medium power microwave	Best cost-effective choice
Silicon	DC circuit – medium/high power	Best choice for high-density fine line interconnections
Aluminum Nitride (AIN)	High power microwave	Ideal CTE match to silicon devices, high thermal conductivity
Beryllia (BeO)	High power DC/RF/microwave	Highest thermal conductivity
Quartz (SiO2)	Microwave/millimeter-wave low power/low shunt capacitance	High density patterns, high voltage, low loss tangent/low CTE, but more costly
Titanates	RF/microwave with high Q	Dielectric properties
Ferrites	Circulators/isolators	Magnetic sensitivity
Sapphire	Millimeter-wave/optical circuits with special electrical or mechanical requirements	Low loss tangent, optical surface finish

Table 1. Uses and benefits of various substrate types

Substrate Characterization

Material	Surface Finish (u" CLA)	Standard Thickness mils (mm)	Available Thickness mils (mm)	Available Sizes inches (mm)	Dielectric Constant ε at 1 MHz	Thermal Conductivity (W/m°C) 25 °C/100 °C	Coefficient Thermal Expansion (ppm)	Tanδ 1 MHz 10 GHz
Quartz	60/40 optical	10, 20 (0.25, 0.5)	5 to 40 (0.12 to 1.0)	3, 5 (75, 125)	3.82	5/2	0.55	0.00002 0.0001
Al_20_3	< 1 pol < 3 asf	10, 15, 25 (0.25, 0.38, 0.63)	5 to 60 (0.12 to 1.0)	4.5 x 3.75 4.5 x 4.5 2 x 2	9.9	35/27	7.4	0.0001 0.0003
AIN	< 3 pol < 24 asf	20, 25, 50 (0.5, 0.63, 1.3)	10 to 85 (0.25 to 2.1)	4.25 x 4.25 (108 x 108)	8.6	170/130	4.6	0.001 0.002
BeO	< 4 pol < 15 asf	15, 25 (0.38, 0.63)	10 to 60 (0.25 to 1.5)	2.9 x 2.3 (74 x 58)	6.5	300/240	9	0.0004
Silicon		10, 15, 25 (0.25, 0.38, 0.63)	10 to 25 (0.25 to 0.63)	3, 5 75, 125		180	3.4	

Table 2. Substrate characterization

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Base Conductor Layout

The second most important parameter in any circuit design is the conductor routing, where current density and conductor impedance can play an important part in the circuit performance. Conductor lines must be designed to withstand the current required. The resistance of that line, especially on signal paths, must be low enough not to create circuit performance issues (see Figure 2). Table 3 summarizes some current limitations for different metals. Table 4 shows some pattern or dimensional limitations that must be considered in the layout. During this phase of the design, layout considerations may also be given for placement of any through holes. Except for filled vias, the size of the holes required depends on the application. Either a plated through-hole conductor or just a hole for pin alignments may be used.

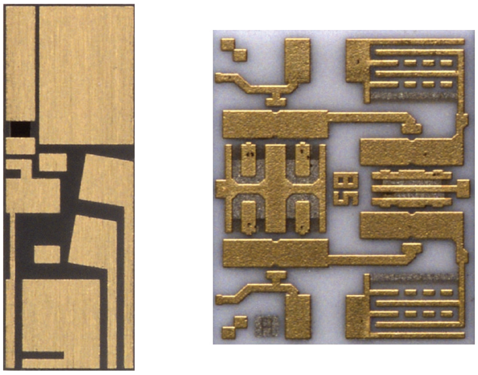


Figure 2. Example of a conductor pattern with special routing for externally mounting components.

Conductor			Wire bonds > 40 mil length (1 mm)		
Conductor Width mils (mm)	Max Current (amps) *		Diameter mils (mm)	Max Current (amps) Gold (Au)	Max Current (amps) Alum Wire (Al)
	Gold	Alum			
1 (0.0254)	0.38	0.075	0.7 (0.170)	0.38	0.28
5 (0.127)	1.9	0.38	1 (0.025)	0.65	0.48
10 (0.254)	3.8	0.76	2 (0.051)	1.83	1.36
15 (0.381)	5.8	1.16	5 (0.013)	~	5.37
20 (0.508)	7.7	1.54	10 (0.245)	~	15.2
25 (0.635)	9.6	5.00	15 (0.381)	~	27.9

*Based on Mil-H-38534 Au at 100 u inches - 25.4 kA thickness; Al at 50 u inches.

Table 3. Base conductor layout

Conductor width	Standard: 0.002" - 0.001 available (0.05 mm to 0.025 mm)
Conductor line thickness	50 to 300 u inches Au (12.7 kA to 76.2 kA) Standard: 0.002 inches Cu Standard: 0.006 available (0.05 mm to 0.15 mm)
Line width tolerance	0.001 inches at 150 u inches (0.025 mm)
Though hole minimum diameter	0.005 inches dependent on substrate thickness (0.125 mm)
Through hole tolerance, diameter, position	± 0.002 inches (0.05 mm)
Metalized hole diameter to thickness ratio	0.8 minimum or greater preferred

Table 4. Pattern and Dimensional Layout Considerations

Thin Film High-Density Integration (HDI) Design Guidelines

Base Resistor Layout

Resistor Range and Sheet Resistance

The choice of resistors is dependent on factors such as resistor material, power, TCR, tolerance, and application. All these factors should be known prior to layout design.. The basic building blocks for any resistor are shown in Figure 4, while Tables 5a, 5b, 5c, and 6 show material options, resistance ranges, and power current density guidelines.

Application such as microwave or simple DC can affect the choice of the layout. Microwave applications are the most restrictive in design format and available resistance values ranges. Fortunately most microwave requirements require lower value resistors.

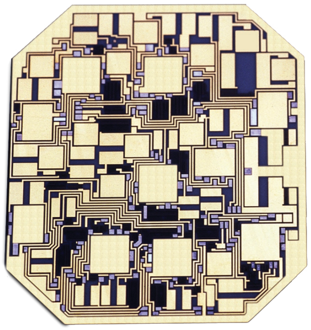
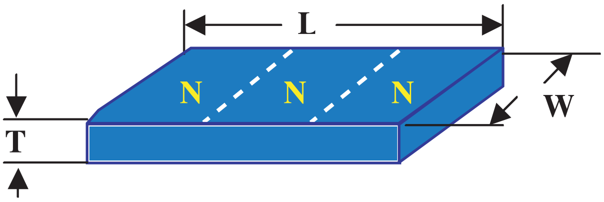


Figure 3. Resistor conductor pattern with 53 resistors for mounting in a special sized package.



N = L/W = Number of squares (three in this case)
P = Intrinsic resistivity in Ω-cm
R_s = Sheet resistance = p/t in Ω / square
R = Resistance p x L/Wt or n x Rs in ohms
R_{max} = A x Rs/W2

Although resistance range varies sheet resistivity, it is determined primarily by pattern geometry. Maximum values attainable is limited by available area (A).

Figure 4. Basic Resistor Building Blocks

Resistor Material		Tantalum Nitride		Nichrome	
Sheet resistance Ω / square	Nom	10 - 50	50 - 100	100 - 200	Standard (10 - 250 custom)
	Sputtered tolerance	± 15%	± 20%	± 30%	± 20%
Absolute TCR PPM/C		± 25, 50	± 100	± 200	± 15, ± 25, ± 50, ± 100

Table 5a. Available film systems

Range	5 ohm to 2 meg
Absolute Tolerance	5% to 0.1%
Ratio Tolerance	1% to 0.01% (range dependent)

Table 5b. Standard resistor parameters

Range	10 ohm to 1 K ohm
Absolute Tolerance	0.5%
Ratio Tolerance	0.5%
Absolute TCR	< = 200 ppm

Table 5c. Microwave resistor parameters

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Sheet Resistance	Al_2O_3	Silicon	Quartz	AIN	BeO
@ 25 ohms/sq	4 ma/mil line width	20 ma/mil line width	0.5 ma/mil line width	19 ma/mil line width	32 ma/mil line width
@ 50 ohms/sq	2 ma/mil line width	10 ma/mil line width	0.25 ma/mil line width	9.5 ma/mil line width	16 ma/mil line width
@ 100 ohms/sq	1 ma/mil line width	5 ma/mil line width	0.125 ma/mil line width	4.7 ma/mil line width	8 ma/mil line width
@ 200 ohms/sq	0.5 ma/mil line width	2.5 ma/mil line width	0.062 ma/mil line width	2.3 ma/mil line width	4 ma/mil line width

Table 6. Power current density vs. material and film selection. The lower the sheet resistivity, the higher the current density.

Microwave Resistor Design

Ideal resistor design for microwave applications evolves from a stripline format where resistor layout is simply a rectangle without any cuts that could cause reflection and affect VSWR characteristics. In practice, unless resistor tolerance is loose, most manufacturers require trimming to maximize yields. To minimize the affects of trimming, utilize edge sense trimming for these resistors around a centerline to maintain frequency response (Figure 5). Current inspection criteria allows up to 50% of the resistor to be removed. The use of a high-temperature stabilization procedure produces very stable resistors and minimizes drift over time or temperature.

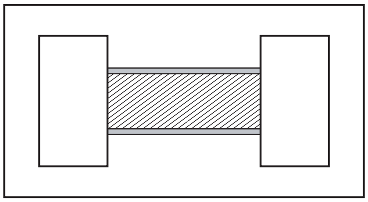

Figure 5. Stripline format for resistor layout.

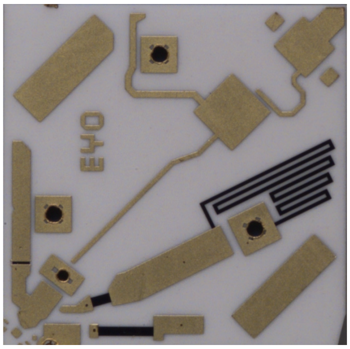

Figure 6. A typical microwave design.

Cutouts and Special Shapes

For many applications it is necessary to have a substrate fit into a particular cavity or allow cutouts for component placement of die planer with the substrate surface. With Co2 cutting, almost any shape from round discs to a complex U shaped structure with multiple hole placements can be achieved (Figure 7).

This technology allows us to do our own in-hole drill for plated through holes, filled vias, edge-wrap metallization, and two sided-substrate patterning.

Parameter	AIN, BeO
Substrates	Alumina, AIN, BeO, Quartz
Position tolerance	± 0.003” (0.076 mm)
Substrate edge to circuit	0.002” min (0.05 mm)
Inside corner radius	0.005” min (0.127 mm)
% of substrate removal	25%

Table 7. Laser machining capability.

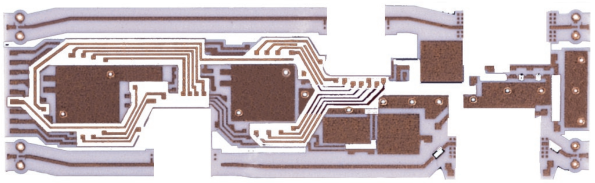

Figure 7. With Co_2 cutting, almost any shape from round discs to a complex U shaped structure with multiple hole placements can be achieved.

Thin Film High-Density Integration (HDI) Design Guidelines

Layers

In general, the size required by the application will determine the number of layers: single, two-sided or multilayer. Applications that limit size are the most demanding to lay out, compelling the designer to use a two-sided or multilayer solution (Figure 7). It's most cost effective to manufacture as a single layer whereeever possible. At this point consideration must be taken for conducter routing, vias, resistor cell, added actve devices, special features such as capacitors, Lange couples and any asociated interconnects. High-density and multilayer design require complexity and a close relationship to end product performance to assure optimum performance. The use of a cad systems can steamline design difficulties. Table 8 lists the various layer applications and metal choices for each. Where mutiple choices exist, compatability with other metals must be analyzed, and choices are given in Table 9.

Figure 8. Typical substrate with combination of thin gold and thick copper/gold areas for solder attach or high-current applications.

Layer	Material	Sputter Thickness	Plated Thickness	Comments
Adhesion	Titanium-Tungsten (TiW)	500 Å min	N/A	
	Titanium (Ti)	500 Å min	N/A	
	Nickel Chromium (NiCr)	500 Å min.	N/A	
	Chrome (Cr)	500 Å min	N/A	
	Tantalum Nitride (Ta_2N)	300 Å min	N/A	
Barrier	Palladium (Pd)	3 kÅ - 5 kÅ	N/A	High temperature barrier
	Titanium Tungsten (TiW)	500 Å min.	N/A	High temperature barrier
	Nickel (Ni)	1.5 kÅ - 5 kÅ	5 kÅ - 15 kÅ	
Conductor	Aluminum (Al)	10 kÅ min	N/A	
	Gold (Au)	1 kÅ - 3 kÅ (4 - 12 u")	25 kÅ min (100 u")	
	Copper (Cu)	N/A	4 kÅ - 11 kÅ (15 - 45 u")	
High Current Conductor	Gold (Au)	N/A	75 kÅ min (300 u")	
	Copper (Cu)	N/A	250 kÅ (0.001")	Available to 0.006"
Dielectric	Silicon Nitride (Si_3N_4)	2 kÅ - 5 kÅ		Dielectric constant = 6.9
	Polyimide	48 kÅ - 49 kÅ		Dielectric constant = 3.4

Table 8. Typical Film Thickness

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Metal stack	Layers: Single, Double, Multi	Maximum Exposure Temperature ºC	Solderable		Wire Bondable	Braze-able
			Gold	Solder		
Ta_2N/TiW/Au	S, D	450			Yes	
Ta_2N/TiW/Au/Ni/Au	S, D	350	Yes	Yes	Yes	Yes
Ta_2N/TiW/Pd/Au	S, D	450	Yes	Yes	Yes	
Ta_2N/Pd/Au	S,D	400	Yes	Yes	Yes	
Ta_2N/Ni/Au	S, D	350		Yes	Yes	
Ta_2N/TiW/Au/Cu/Au	S, D	300			Yes	
Ta_2N/TiW/Au/Cu/Ni/Au	S, D, M	300	Yes	Yes	Yes	Yes
NiCr/Au	S, M	350			Yes	
NiCr/TiW/Au	S, D	400			Yes	
NiCr/Au/Ni/Au	S, D	350	Yes	Yes	Yes	
NiCr/Ni/Au	S, D	350	Yes	Yes	Yes	
TiW/Au	S, D, M	400			Yes	
TiW/Au/Ni/Au	S, D	350	Yes	Yes	Yes	
TiW/Pd/Au	S, D	400	Yes	Yes	Yes	
Ti/Pd/Au	S, D, M	350	Yes	Yes	Yes	
Cr/Ni/Au	S, D, M	350	Yes	Yes	Yes	

Table 9. Metal stack options.

Selecting Through-Hole Vias

The choice between plated through-hole vias and filled vias is a matter of application. The least expensive choice is the plated through-hole, where only a simple front-to-back electrical path is required.

Filled vias are often the choice when improved thermal conductivity to the backside is needed. They offer the designer as many heat channels as the area allows. A filled via also allows the component engineer to place components directly over the via for maximum heat transfer from the component. Filled vias can be used to provide additional low thermal conductivity paths to ground plate heat sinks to improve signal transmission.

Through-hole patterns require a minimum of a 0.005 mils ring around each hole to compensate for the tolerance build-up caused by hole placement, manufacturing alignment, diameter tolerances, the slight laser entrance hole rounding, and other factors (see Figure 9).

Plated through-hole designs require a 0.8 x substrate thickness minimum with typical impedance of less than 20 milliohms (Figure 9). Filled vias require a diameter of 7 ± 2 mils (0.18 ± 0.05 mm) with typical impedance of less than 3 milliohms. With Co_2 cutting, almost any shape from round discs to a complex U shaped structure with multiple hole placements can be achieved.

Edge wraparound connections are also another option to consider when designing connections to backside plane.

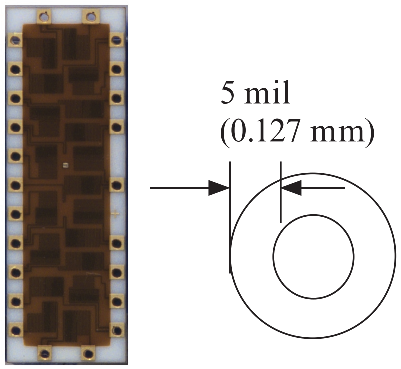

Figure 9. Example of custom resistor network with 19 resistors, 24 plated through-holes and backside metal lands for surface-mount high-voltage application.

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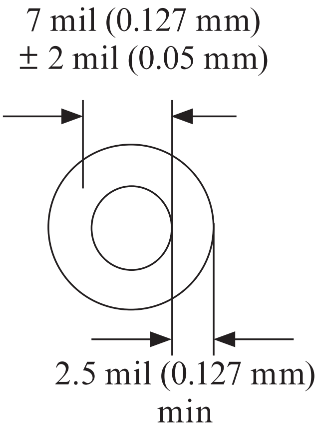

Figure 10. Filled vias.

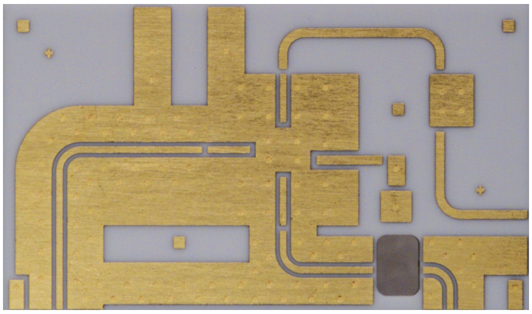

Figure 11. Example of conductor pattern with filled vias.

Air or Polyimide Suport Bridges and Lange Couplers

When crossovers are necessary, air bridges can be configured on the conductor pattern. A sacrificial layer is deposited and patterned before the second layer is put in place. The intermediate layer is then removed leaving the complete air bridge. The same process can be done for a supported air bridge using polyimide; in this case, the polyimide layer remains in place on the finished part. Bridges supported by polyimide provide a more rugged structure.

Dimensional limits are as follows:

Minimum gap between lines: 0.5 mils (0.0127 mm)
Tolerance: ± 0.1 mil (0.00254 mm)

Minimum line width: 0.5 mil (0.0127 mm)
Tolerance: ± 0.1 mil (0.00254 mm)

Bridge height: 300 - 500 u inches

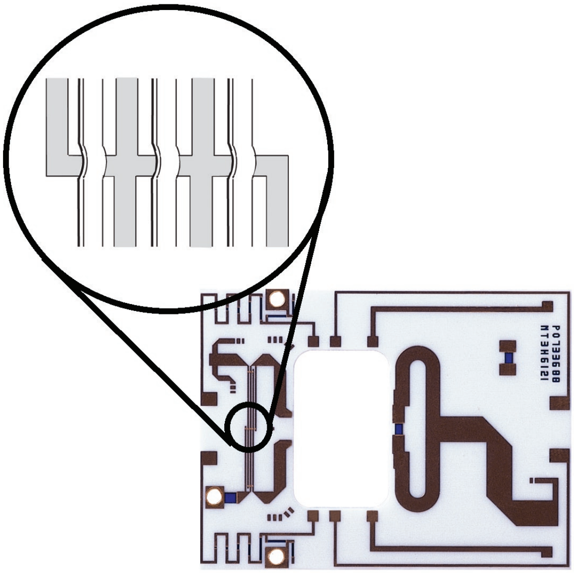

Figure 12. An example of polymide support bridge.

Solder Dam

For many applications the need arises to place components on the substrate with epoxy, or with solder, if tight planerization is needed. This is true particularly in fiber optic sub-mount assemblies. Solder dams can be offered as either polyimide or a lower temperature thermal set plastic.

Backside Layout

Conductor interconnect patterns or ground plane definition can be provided on the bottom surface of the substrate. Front-to-back alignment can be held to 0.002 inches (0.051mm). The backside metallization can also provide shielding for inter conductor layers in multilayer designs. The design shown in Figure 13 combines several feature available using thin film techniques with the backside pattern options: metalized through holes for grounding, large area metal for low impedance, and a custom shape. Backside patterning allows designer a cost-effective alternative to a top-surface multilayer design.

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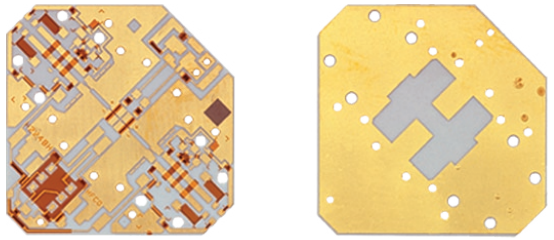

Figure 13. Front and backside patterned array.

The board space saved by taking this approach is summarized in Table 11. This is an approximation since there are many factors that can affect area usage.

Usually no stacking restrictions apply when using the dielectrics listed in Table 10. However, process compatibility issues between layers may restrict the use of multiple metal stacks on multiple dielectric layers. The easiest way to determine your option is to forward what you think is needed and the engineering staff will review it.

Multi-Layer

For designs that require more layers than the single-layer front or back combination can offer, the designer may stack layers on either side in a multilayer arrangement. The use of dielectric material such as polyimide or silicon nitride as an insulating layer between metal layers becomes a primary concern, as shown in Table 10. The most commonly used is polyimide because of its patterning properties and processing temperatures.

Layer	Material	Standard Thickness	Dielectric Constant
Dielectric	Polyimide	2 kΩ - 5 kΩ	6.9
	Silicon Nitride	48 kΩ ± 1 kΩ	3.4

Table 10. Dielectric parameter.

The board space saved by taking this approach is summarized in Table 11. This is an approximation since there are many factors that can affect area usage.

Usually, no stacking restrictions apply when using the dielectrics listed in Table 10. However, process compatibility issues between layers may restrict the use of multiple metal stacks on multiple dielectric layers. The easiest way to determine your option is to forward what you think is needed and the engineering staff will review it.

Multilayer Area Savings Chart Per Layer	
# of layers	Approximate area factor reduction
1	1.33
2	1.77
3	2.37
4	3.16

Table 11. Area savings per layer.

An actual design from a military helicopter used almost

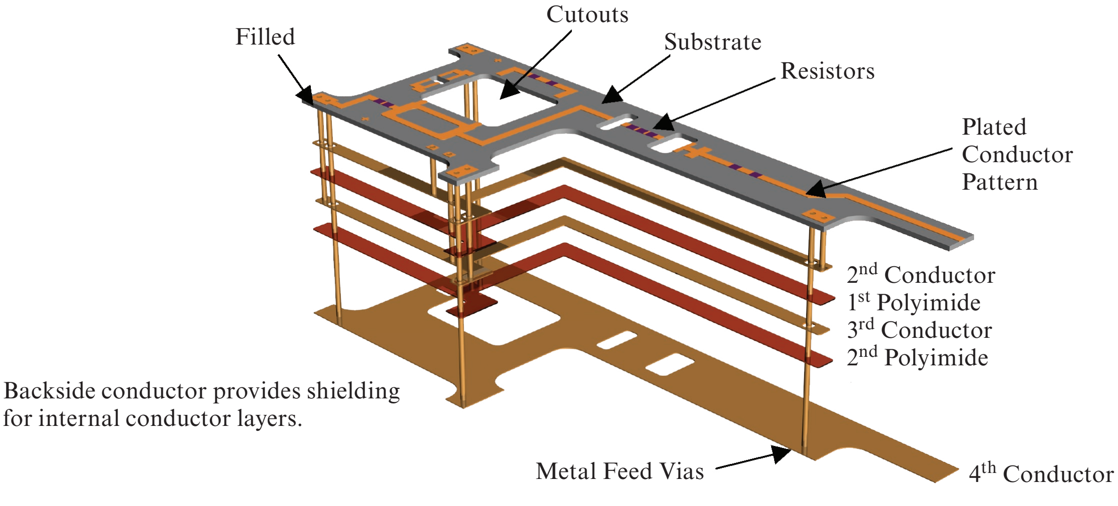

Figure 14. Expanded view of a Thin Film Multilayer HDI circuit.

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all the design/process option available and after significant R&D effort was manufactured with reasonable yields (Figure 14).

Cad Design and Layout

Except for microwave applications where sophisticated circuit modeling is required, Vishay can develop passive circuit layout based on inputs received in schematic format or from rough outline drawings.

The minimum information needed is detailed in the list below. Vishay can also offer hybrid design layout services if parts lists are available.

Design Inputs
Schematic or layout
Minimum/maximum substrate size
Resistor tolerances/ratio tolerances
TCR/TC track
Power per resistor
Metallization preference

Summary

Many issues affect the layout of complex designs. To achieve the best balance for your application, differences in material, size, and performance must be taken into account and reflected in the specification and final layout. It is recommended to work closely with your manufacturer to establish a balanced workable design and to consider all the critical process criteria. When properly designed overall quality and performance can be enhanced to accomplish your goals.

The guideline shown in Figure 15 summarizes the layout design criteria.

References

Thin Film Technology Handbook. Aicha A.R. Elshabini-Riad, Fred D. Bartlow III, McGraw Hill 1998.

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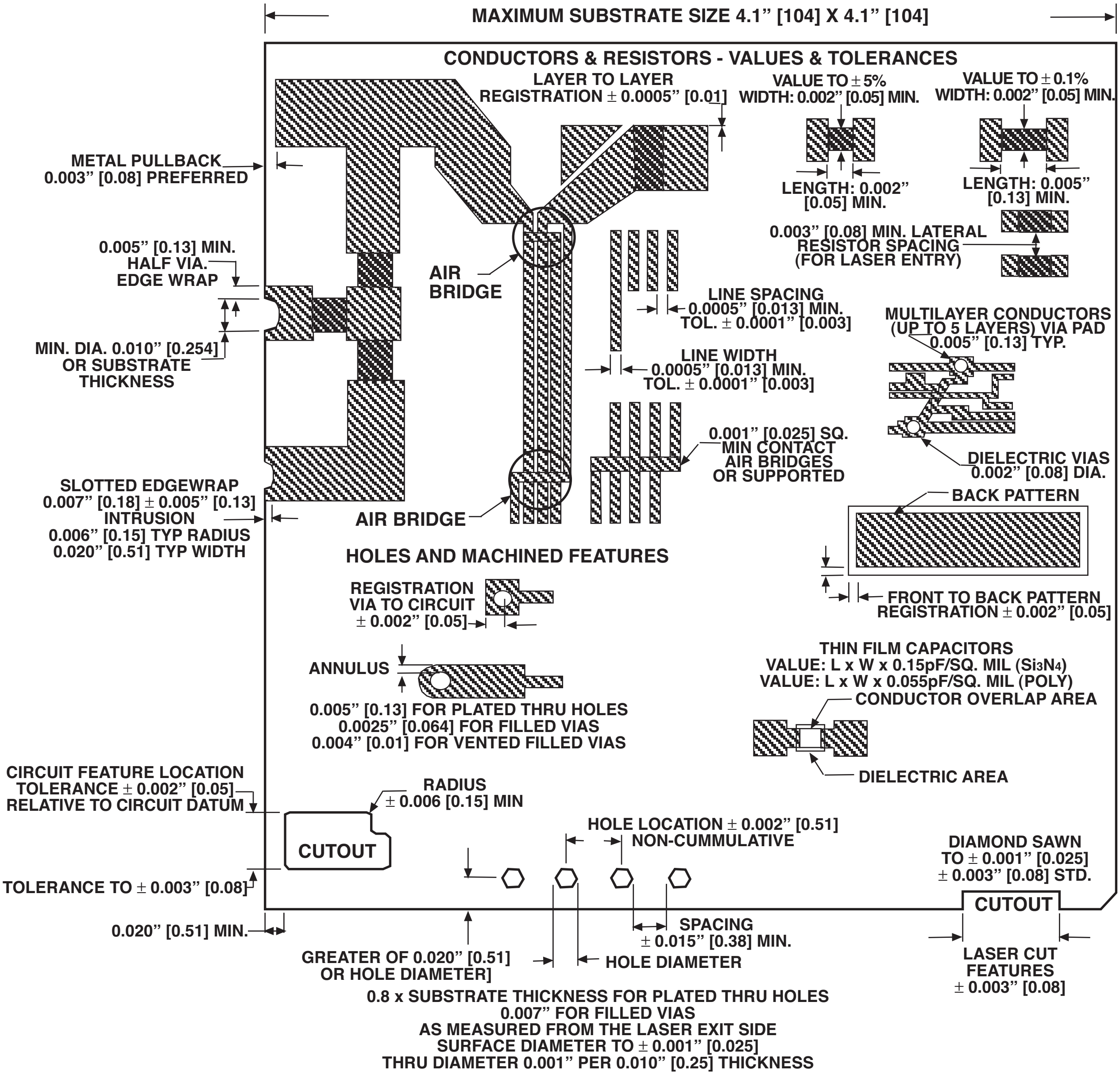

Figure 15. Standard layout guidellines.

http://www.vishay.com/doc?61081

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